

INDIAN MARITIME UNIVERSITY
(A Central University, Government of India)

B.Tech. (Marine Engineering)
Semester – III – December 2015 End Semester Examinations

Electronics
Subject Code: UG11T2302/UG11T1302

Time: 3 Hours
Date: 11.12.2015

Max Marks: 100
Pass Marks: 50

PART- A

(3 x 10 = 30 Marks)

Compulsory Questions

1. a. What are *Universal Gates*? Why they are called universal gate?
- b. With neat circuit diagram explain the working of an *Integrator* using *OPAMP*
- c. Discuss with circuit diagram and truth table working of *Half Adder*
- d. What are the characteristics of an ideal OPAMP
- e. What are the differences between FET and MOSFET?
- f. Solve the following *K-Map* to get solution in *SOP* form

w x \ y z	y z			
	00	01	11	01
00	1	1	X	1
01	1	1	1	0
11	1	0	0	1
01	0	0	1	1

- g. What are the differences between Positive and negative feedback?
- h. What are the advantages of self biased circuit over the fixed biased circuit for an amplifier?
- i. What are basic differences between frequency modulation and phase modulation?
- j. What will be the gain in dB of a two stage R-C coupled cascade amplifier where each stage of amplifier gain is A1?

PART – B

(5 x 14 = 70 Marks)

Answer any five from the following questions

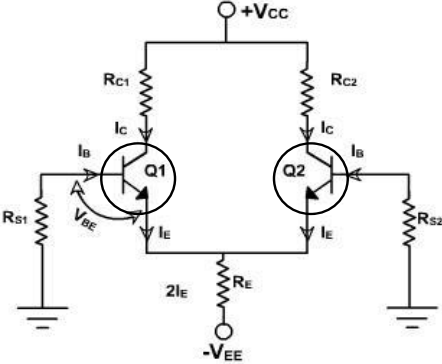
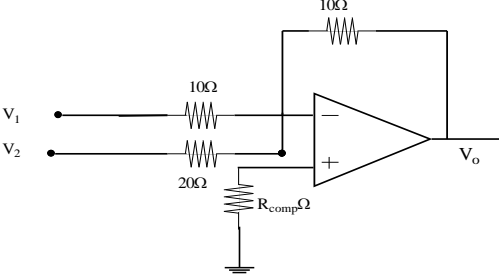
2. a. Realize a 3 bit Adder circuit and explain its operation
- b. Optimize the given function

$$f(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 11, 13, 15)$$

7

7

3.
 - a. For a transistor prove that collector current 6

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$
 Where β is the CE current gain, I_B is the base current and I_{CBO} is the collector to base leakage current.
 - b. Draw and explain Class A and Class B power amplifier. 4
 - c. Explain Load Line 4
4.
 - a. Obtain the operating point (I_{CQ} and V_{CEQ}) for Differential Amplifier given below 7

 - b. Find the output voltage V_o of the circuit shown below. 7

5.
 - a. Describe the construction and working principle of a FET 4
 - b. A transistor amplifier has a voltage gain of 50. The input resistance of the amplifier is 1 K ohm and the output resistance is 40 K ohms. The amplifier is now provided with 10 % negative voltage feed back in series with the input. Calculate the voltage gain, input and output resistance with feedback. 6
 - c. Draw and explain *Tuned Oscillator*. 4
6.
 - a. Prove that in amplitude modulation (AM) total carrier power 6

$$P_t = P_c (1 + m_a^2/2).$$
 Where P_c is the carrier power and m_a is the modulation index.
 - b. Explain any amplitude demodulation circuit. 4
 - c. A Broadcast transmitter radiates 5 KW when the percentage modulation is 50%. Calculate the total carrier power when the modulation has been reduced to 30 %. 4
7.
 - a. Draw and explain a Push Pull Amplifier 6
 - b. How frequency can measure using CRO 4
 - c. Briefly Explain Super Heterodyne Receiver for wireless communications 4

8.

- a. Define *Resolution, Linearity* of a *Digital to Analog Convertor* 4
- b. With neat diagram explain the operation of *CMOS Inverter* (NOT gate). 4
- c. Explain the operation of *D flip-flop*. Show the truth table and timing diagram. 4
- d. State the operation the following instruction of 8085 microprocessor will perform
i. MOV r_1, r_2 2
